TSL202R

128 × 1 Linear Sensor Array

General Description

The TSL202R linear sensor array consists of two sections of 64 photodiodes and associated charge amplifier circuitry arranged to form a contiguous 128 × 1 array. The pixels measure 120µm (H) by 70µm (W) with 125µm center-to-center spacing and 55µm spacing between pixels. Operation is simplified by internal control logic that requires only a serial-input (SI) signal and a clock.

The TSL202R is intended for use in a wide variety of applications including mark detection and code reading, optical character recognition (OCR) and contact imaging, edge detection and positioning as well as optical linear and rotary encoding.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of the TSL202R, 128x1 Linear Sensor Array are listed below:

Figure 1:
Added Value of Using TSL202R

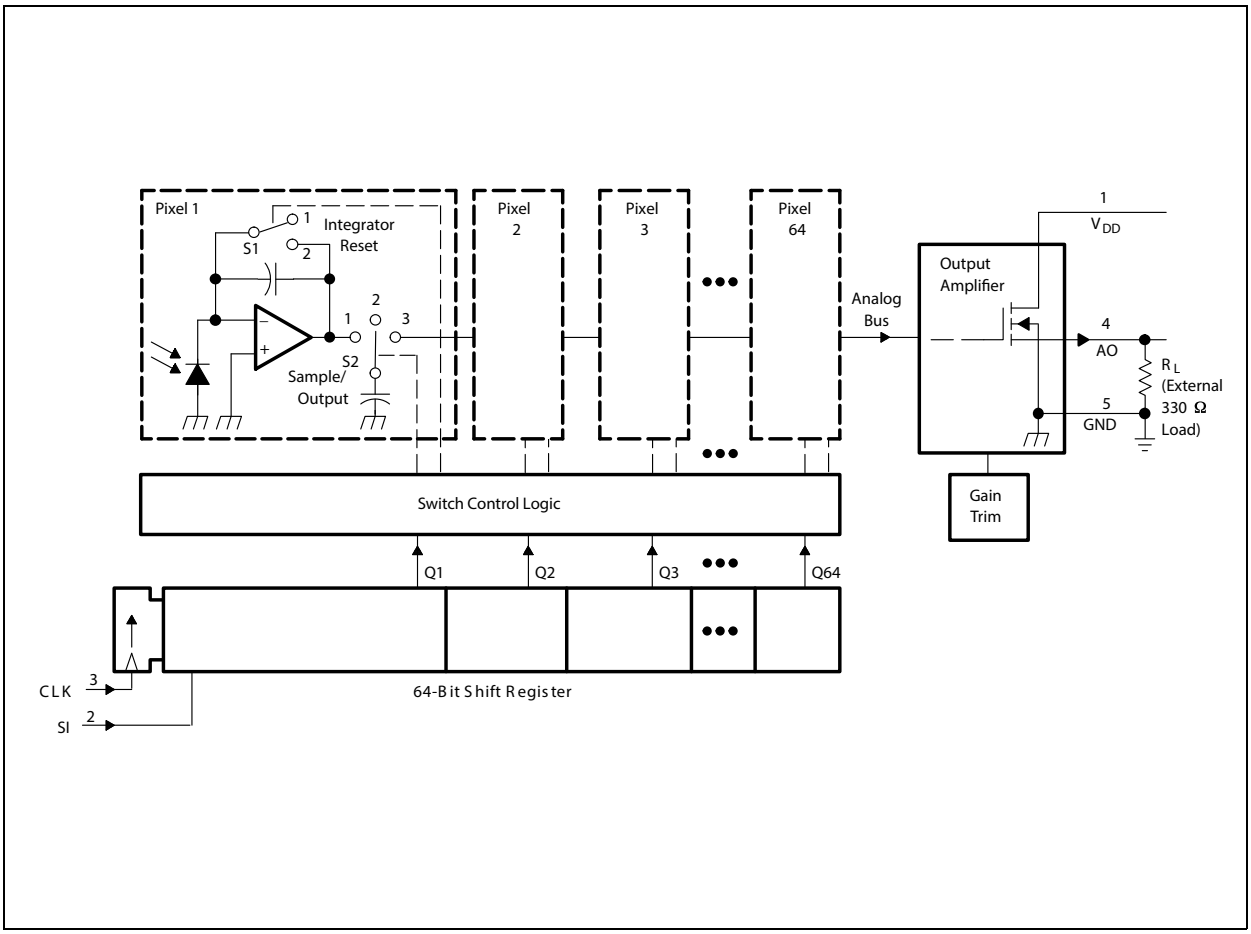
Benefits	Features
• Provides High Density Pixel Count	• 128 x 1 Sensor-Element Organization
• Enables High Resolution Scanning	• 200 Dots-Per-Inch (DPI) Sensor Pitch
• Enables Capacitive Threshold Sensing	• High Linearity and Uniformity
• Provides Full Dynamic Range	• Rail-to-Rail Output Swing

- Wide Dynamic Range: 2000:1 (66dB)
- Output Referenced to Ground
- Low Image Lag: 0.5% Typical
- Operation to 5MHz
- Single 5V Supply
- Replacement for TSL202

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TSL202R Block Diagram (each section - pin numbers apply to section 1)



Pin Assignments

The TSL202R pin assignments are described below:

Figure 3:
Pin Diagram (Top View)

Pin Diagram:
NC - No internal connection

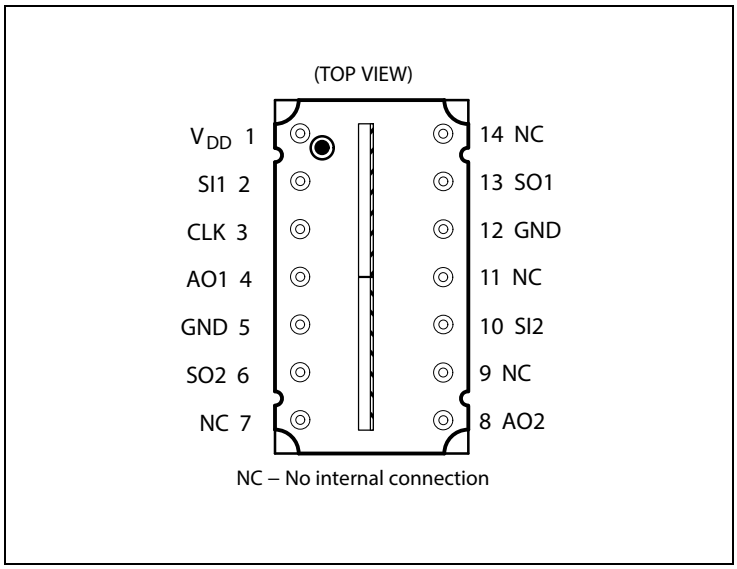


Figure 4:
Pin Description

Terminal		Description
Name	No.	
V_{DD}	1	Supply voltage. Supply voltage for both analog and digital circuitry.
SI1	2	Serial input (section 1). SI1 defines the start of the data-out sequence.
CLK	3	Clock. Clk controls charge transfer, pixel output, and reset.
AO1	4	Analog output of section 1
GND	5, 12	Ground (substrate). All voltages are referenced to GND.
SO2	6	Serial output (section 2). SO2 provides a signal to drive the SI input of another device for cascading or as an end-of-data indication.
NC	7, 9, 11, 14	No internal connection
AO2	8	Analog output of section 2
SI2	10	Serial input (section 2). SI2 defines the start of the data-out sequence.
SO1	13	Serial output (section 1). SO1 provides a signal to drive the SI2 input.

Detailed Description

The sensor consists of 128 photodiodes arranged in a linear array. Light energy impinging on a photodiode generates photocurrent, which is integrated by the active integration circuitry associated with that pixel. During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity and the integration time. The integration time is the interval between two consecutive output periods.

The output and reset of the integrators is controlled by a 128-bit shift register and reset logic. An output cycle is initiated by clocking in a logic 1 on SI for one positive going clock edge (see Figure 10 and Figure 11)[1]. As the SI pulse is clocked through the 128-bit shift register, the charge on the sampling capacitor of each pixel is sequentially connected to a charge-coupled output amplifier that generates a voltage output, AO. When the bit position goes low, the pixel integrator is reset. On the 129^{th} clock rising edge, the SI pulse is clocked out of the shift register and the output assumes a high-impedance state. Note that this 129^{th} clock pulse is required to terminate the output of the 128^{th} pixel and return the internal logic to a known state. A subsequent SI pulse can be presented as early as the 130^{th} clock pulse, thereby initiating another pixel output cycle.

The voltage developed at analog output (AO) is given by:

(EQ1) $$V_{out} = V_{drk} + (R_e)\,(E_e)\,(t_{int})$$

where:

- V_{out} is the analog output voltage for white condition
- V_{drk} is the analog output voltage for dark condition
- R_e is the device responsivity for a given wavelength of light given in $V/(\mu J/cm^2)$
- E_e is the incident irradiance in $\mu W/cm^2$
- t_{int} is integration time in seconds

AO is driven by a source follower that requires an external pulldown resistor (330Ω typical). The output is nominally 0V for no light input, 2V for normal white-level, and 3.4V for saturation light level. When the device is not in the output phase, AO is in a high impedance state.

A 0.1µF bypass capacitor should be connected between V_{DD} and ground as close as possible to the device.

1. For proper operation, after meeting the minimum hold time condition, SI must go low before the next rising edge of the clock.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage range	-0.3	6	V
V_I	Input voltage range	-0.3	V_{DD} + 0.3V	V
I_{IK}	Input clamp current, (V_I < 0) or (V_I > V_{DD})	-20	20	mA
I_{OK}	Output clamp current, (V_O < 0) or (V_O > V_{DD})	-25	25	mA
V_O	Voltage range applied to any output in the high impedance or power-off state	-0.3	V_{DD} + 0.3V	V
I_O	Continuous output current, (V_O = 0 to V_{DD})	-25	25	mA
	Continuous current through V_{DD} or GND	-40	40	mA
I_O	Analog output current range	-25	25	mA
T_A	Operating free-air temperature range	-25	85	°C
T_{STRG}	Storage temperature range	-25	85	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		260	°C
ESD_{HBM}	ESD tolerance, human body model	±2000		V

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions (see Figure 10 and Figure 11)

Symbol	Parameter	Min	Nom	Max	Unit
V_{DD}	Supply voltage	4.5	5	5.5	V
V_I	Input voltage	0		V_{DD}	V
V_{IH}	High-level input voltage	2		V_{DD}	V
V_{IL}	Low-level input voltage	0		0.8	V
λ	Wavelength of light source	400		1000	nm
f_{clock}	Clock frequency	5		5000	kHz
t_{int}	Sensor integration time, serial	0.026		100	ms
t_{int}	Sensor integration time, parallel	0.013		100	ms
T_A	Operating free-air temperature	0		70	°C
R_L	Load resistance	300		4700	Ω
C_L	Load capacitance			420	pF

Figure 7:
Electrical Characteristics at f_{clock} = 1MHz, V_{DD} = 5V, T_A = 25°C, λ_p = 640nm, t_{int} = 5ms, R_L = 330Ω, E_e = 16.5µW/cm^2 (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{out}	Analog output voltage (white, average over 128 pixels)	See note (1)	1.6	2	2.4	V
V_{drk}	Analog output voltage (dark, average over 128 pixels)		0	50	150	mV
PRNU	Pixel response nonuniformity	See note (2) and See note (3)		±4%	±10%	
	Nonlinearity of analog output voltage	See note (3)		±0.4%		FS
	Output noise voltage	See note (4)		1		mVrms
R_e	Responsivity		18	23	30	V/(µJ/cm^2)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SE	Saturation exposure	See note (5)		142		nJ/cm^2
V_{sat}	Analog output saturation voltage		2.5	3.4		V
DSNU	Dark signal nonuniformity	All pixels (6)		25	120	mV
IL	Image lag	See note (7)		0.5%		
I_{DD}	Supply current, output idle			7	10	mA
I_{IH}	High-level input current	$V_I = V_{DD}$			10	µA
I_{IL}	Low-level input current	$V_I = 0$			10	µA
V_{OH}	High-level output voltage, SO1 and SO2	$I_O = 50µA$	4.5	4.95		V
		$I_O = 4mA$		4.6		
V_{OL}	Low-level output voltage, SO1 and SO2	$I_O = 50µA$		0.01	0.1	V
		$I_O = 4mA$		0.4		
$C_{i(SI)}$	Input capacitance, SI			5		pF
$C_{i(CLK)}$	Input capacitance, CLK			10		pF

Note(s):

1. The array is uniformly illuminated with a diffused LED source having a peak wavelength of 640nm.
2. PRNU is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated at the white irradiance level. PRNU includes DSNU.
3. Nonlinearity is defined as the maximum deviation from a best-fit straight line over the dark-to-white irradiance levels, as a percent of analog output voltage (white).
4. RMS noise is the standard deviation of a single-pixel output under constant illumination as observed over a 5-second period.
5. Minimum saturation exposure is calculated using the minimum Vsat, the maximum Vdrk, and the maximum Re.
6. DSNU is the difference between the maximum and minimum output voltage in the absence of illumination.
7. Image lag is a residual signal left in a pixel from a previous exposure. It is defined as a percent of white-level signal remaining after a pixel is exposed to a white condition followed by a dark condition:

$$IL = \frac{V_{out(IL)} - V_{drk}}{V_{out(white)} - V_{drk}} \times 100$$

Figure 8:
Timing Requirements (see Figure 10 and Figure 11)

Symbol	Parameter	Min	Nom	Max	Unit
$t_{su(SI)}$	Setup time, serial input (1)	20			ns
$t_{h(SI)}$	Hold time, serial input (1), (2)	0			ns
t_w	Pulse duration, clock high or low	50			ns
t_r , t_f	Input transition (rise and fall) time	0		500	ns

Note(s):

1. Input pulses have the following characteristics: t_r = 6ns, t_f = 6ns.
2. SI must go low before the rising edge of the next clock pulse.

Figure 9:
Dynamic Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (see Figure 11)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_s	Analog output settling time to ±1%	R_L = 330Ω, C_L = 10pF		185		ns
$t_{pd(SO)}$	Propagation delay time, SO1, SO2			50		ns

Typical Characteristics

Figure 10:
Timing Waveforms

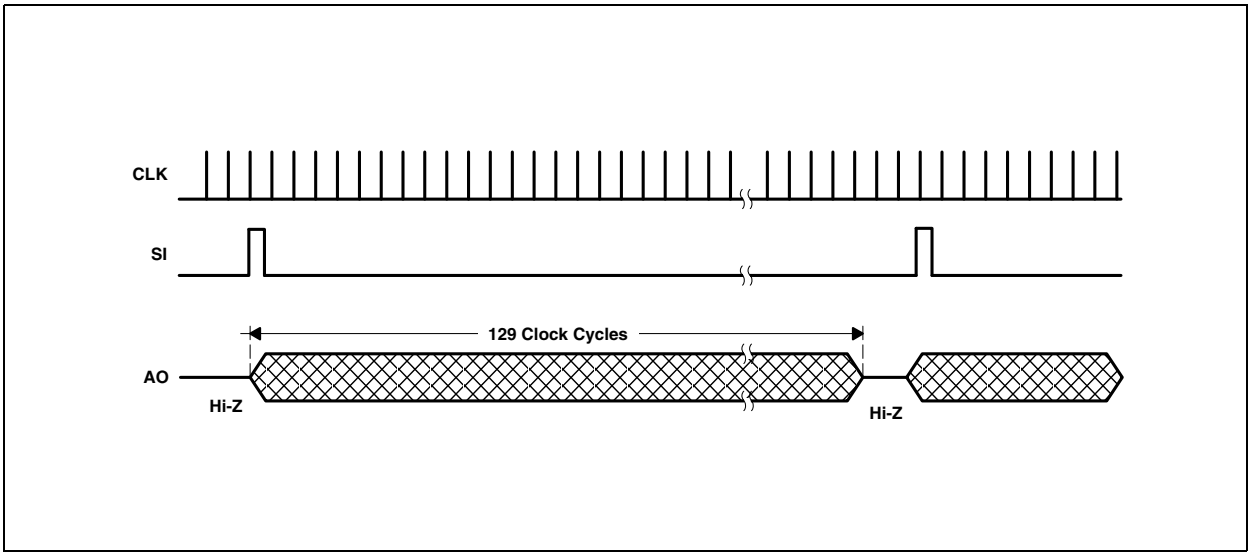


Figure 11:
Operational Waveforms (each section)

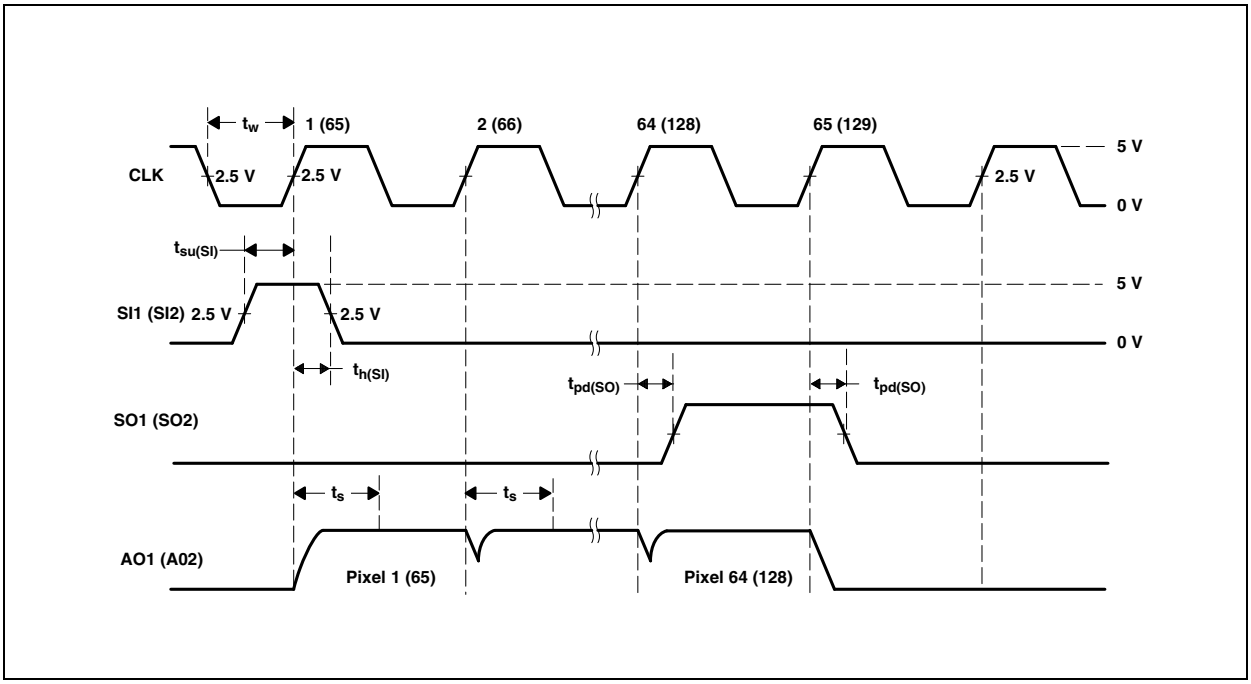


Figure 12:
Photodiode Spectral Responsivity

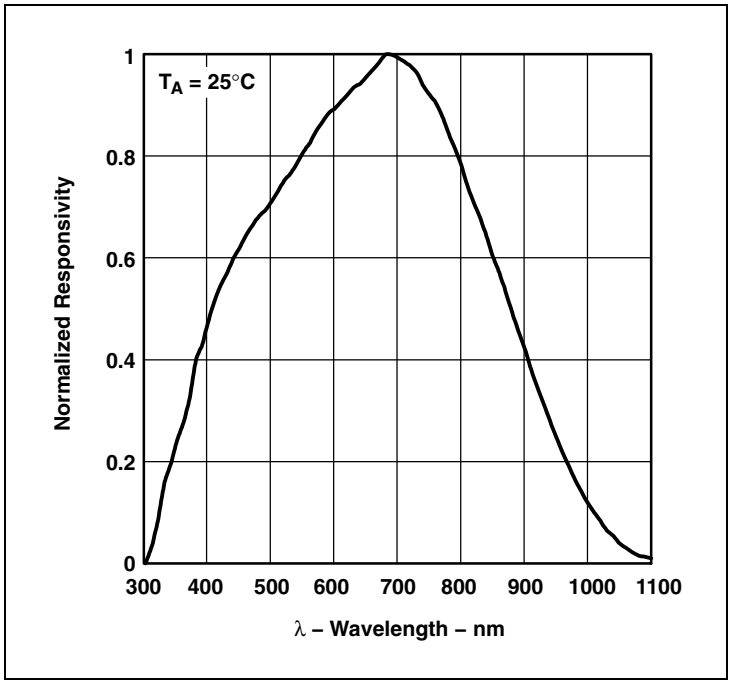
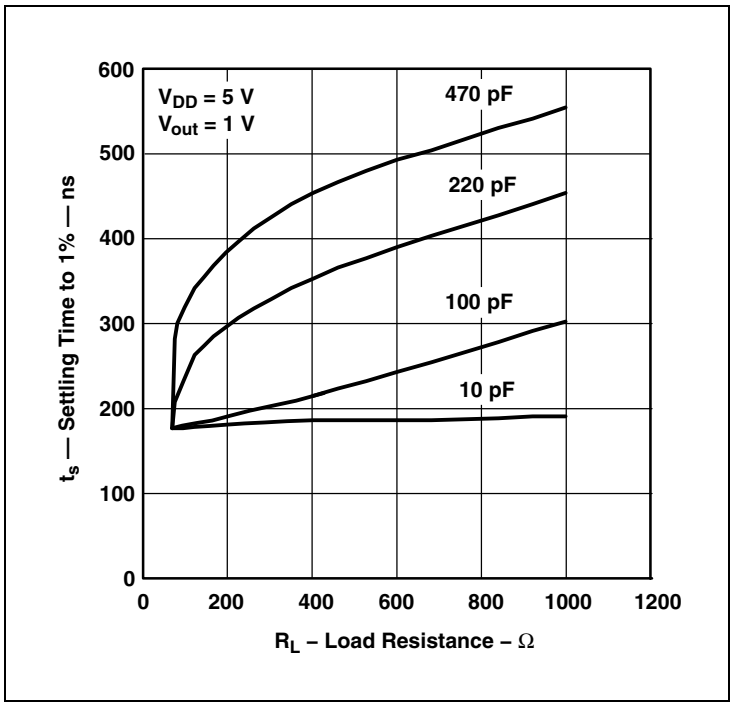


Figure 13:
Analog Output Settling Time vs. Load Capacitance and Resistance



Application Information

Power Supply Considerations

For optimum device performance, power-supply lines should be decoupled by a 0.01µF to 0.1µF capacitor with short leads mounted close to the device package
(see Figure 14 and Figure 15).

Integration Time

The integration time of the linear array is the period during which light is sampled and charge accumulates on each pixel's integrating capacitor. The flexibility to adjust the integration period is a powerful and useful feature of the **ams** TSL2xx linear array family. By changing the integration time, a desired output voltage can be obtained on the output pin while avoiding saturation for a wide range of light levels.

Each pixel of the linear array consists of a light-sensitive photodiode. The photodiode converts light intensity to a voltage. The voltage is sampled on the Sampling Capacitor by closing switch S2 (position 1) (see Figure 2). Logic controls the resetting of the Integrating Capacitor to zero by closing switch S1 (position 2).

At SI input (Start Integration), pixel 1 is accessed. During this event, S2 moves from position 1 (sampling) to position 3 (holding). This holds the sampled voltage for pixel 1. Switch S1 for pixel 1 is then moved to position 2. This resets (clears) the voltage previously integrated for that pixel so that pixel 1 is now ready to start a new integration cycle. When the next clock period starts, the S1 switch is returned to position 1 to be ready to start integrating again. S2 is returned to position 1 to start sampling the next light integration. Then the next pixel starts the same procedure. The integration time is the time from a specific pixel read to the next time that pixel is read again. If either the clock speed or the time between successive SI pulses is changed, the integration time will vary. After the final (n^{th}) pixel in the array is read on the output, the output goes into a high-impedance mode. A new SI pulse can occur on the (n+1) clock causing a new cycle of integration/output to begin. Note that the time between successive SI pulses must not exceed the maximum integration time of 100msec.

The minimum integration time for any given array is determined by time required to clock out all the pixels in the array and the time to discharge the pixels. The time required to discharge the pixels is a constant. Therefore, the minimum integration period is simply a function of the clock frequency and the number of pixels in the array. A slower clock speed increases the minimum integration time and reduces the maximum light level for saturation on the output. The minimum integration time shown in this data sheet is based on the maximum clock frequency of 5MHz.

The minimum integration time can be calculated from the equation:

(EQ2) $$T_{int(min)} = \left(\frac{1}{maximum\ clock\ frequency}\right) \times n$$

where:

n is the number of pixels

In the case of the TSL202R, the minimum integration time would be:

$T_{int(min)} = 200ns \times 128 = 25.6\mu s$

It is important to note that not all pixels will have the same integration time if the clock frequency is varied while data is being output.

It is good practice on initial power up to run the clock (*n*+1) times after the first SI pulse to clock out indeterminate data from power up. After that, the SI pulse is valid from the time following (*n*+1) clocks. The output will go into a high-impedance state after the *n*+1 high clock edge. It is good practice to leave the clock in a low state when inactive because the SI pulse required to start a new cycle is a low-to-high transition.

The integration time chosen is valid as long as it falls in the range between the minimum and maximum limits for integration time. If the amount of light incident on the array during a given integration period produces a saturated output (Max Voltage output), then the data is not accurate. If this occurs, the integration period should be reduced until the analog output voltage for each pixel falls below the saturation level. The goal of reducing the period of time the light sampling window is active is to lower the output voltage level to prevent saturation. However, the integration time must still be greater than or equal to the minimum integration period.

If the light intensity produces an output below desired signal levels, the output voltage level can be increased by increasing the integration period provided that the maximum integration time is not exceeded. The maximum integration time is limited by the length of time the integrating capacitors on the pixels can hold their accumulated charge. The maximum integration time should not exceed 100ms for accurate measurements.

Although the linear array is capable of running over a wide range of operating frequencies up to a maximum of 5MHz, the speed of the A/D converter used in the application is likely to be the limiter for the maximum clock frequency. The voltage output is available for the whole period of the clock, so the setup and hold times required for the analog-to-digital conversion must be less than the clock period.

Connection Diagrams

Figure 14:
Serial Connection

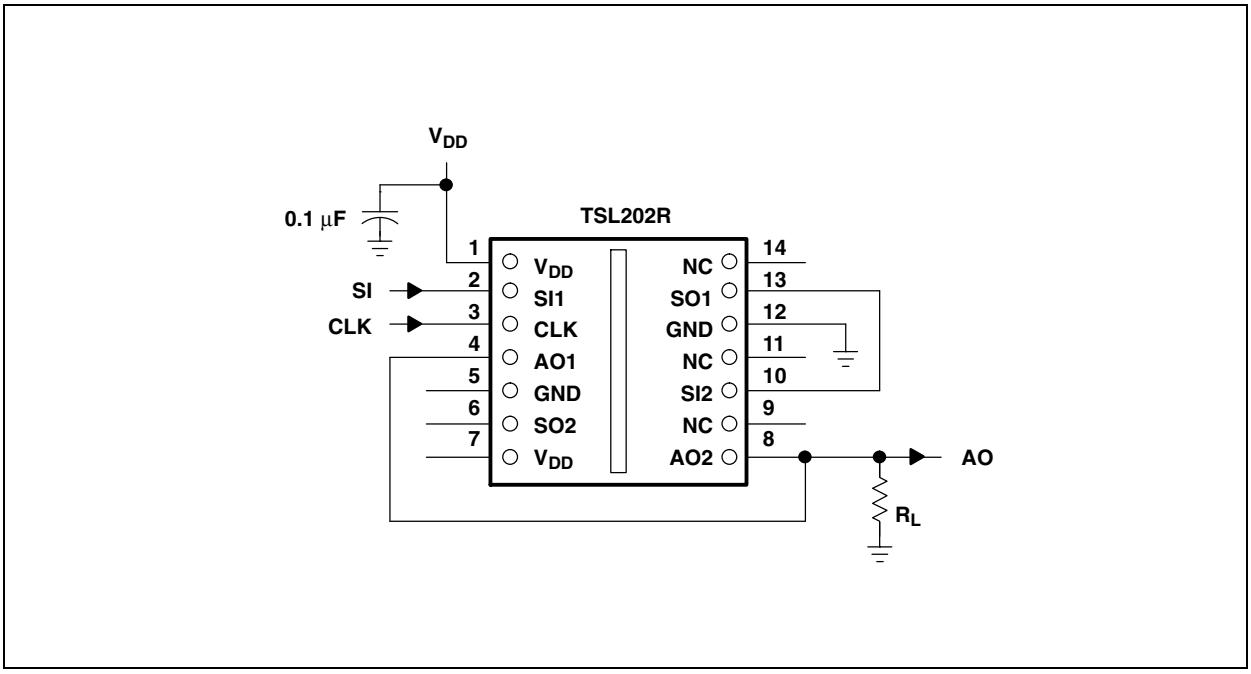
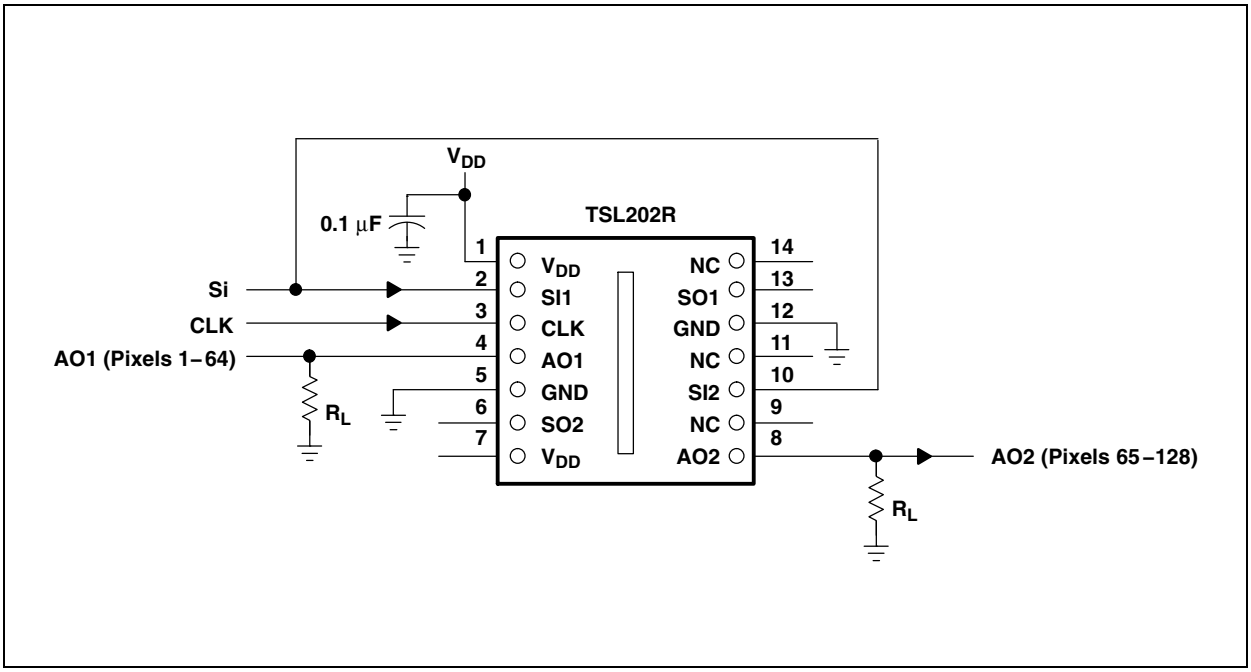


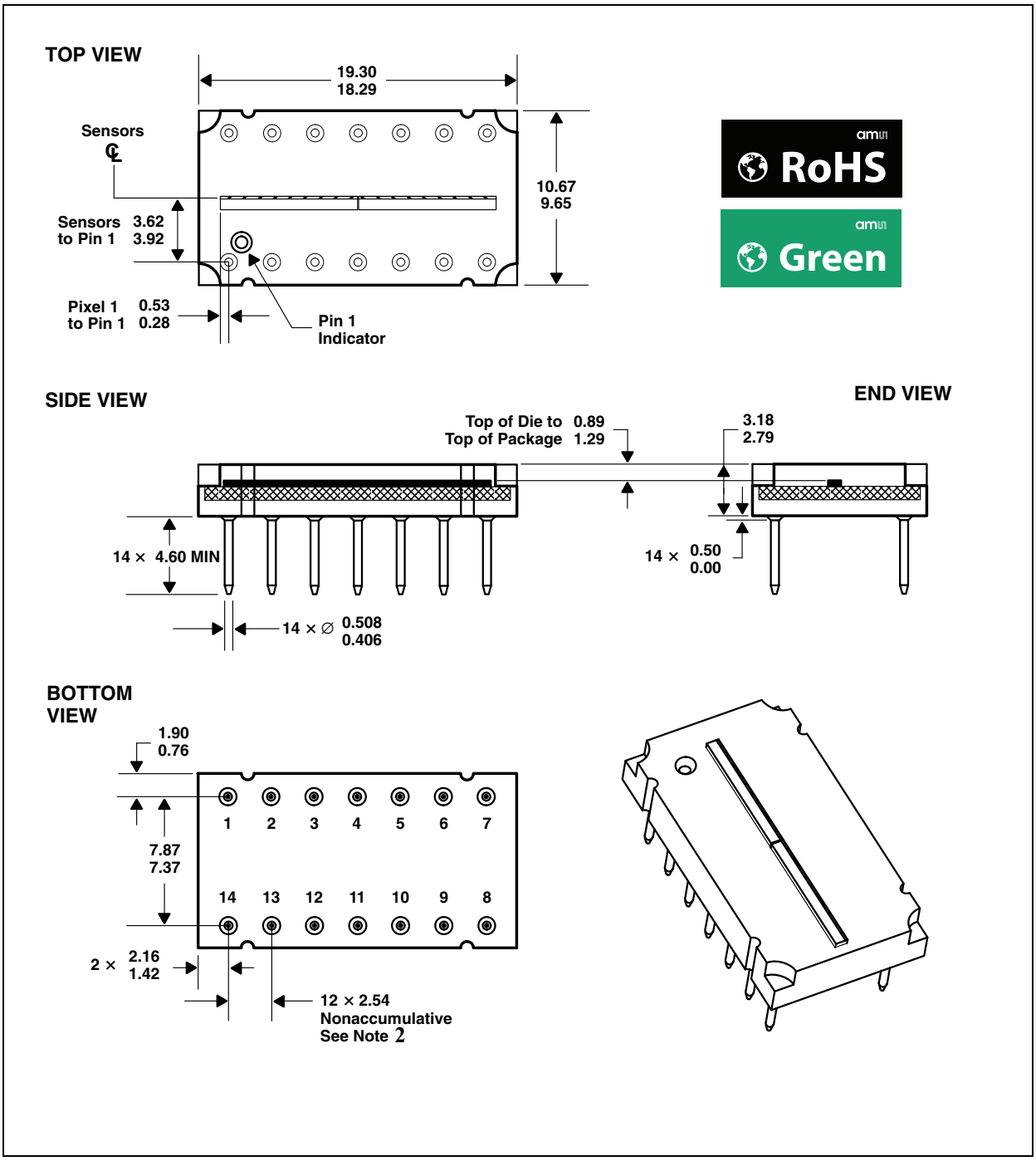
Figure 15:
Parallel Connection



Mechanical Information

This assembly consists of 2 sensor chips mounted on a printed-circuit board in a clear molded plastic package.

Figure 16:
TSL202R Solder Bump Linear Array Package



Note(s):

1. All linear dimensions are in millimeters.
2. The true-position spacing is 2.54mm between lead centerlines. Each pin centerline is located within 0.25mm of its true longitudinal positions.
3. Index of refraction of clear plastic is 1.52.
4. This drawing is subject to change without notice.

Soldering Information

TSL202 128 x 1 linear array 14-lead gold pin package soldering instructions:

- The TSL202R has been designed to withstand a lead temperature during soldering of 260°C for 10 seconds at a distance of 1.6mm from the package body.
- In most applications, these *through-hole* parts will be sufficiently protected by the combination of the PCB or flex plus the standoff provided by the package.
- If lead clipping is required, this should be performed after solder attach to prevent the pulling of the lead from the package body.
- As in all board manufacturing, care should be taken to prevent part bending during board singulation or final assembly.
- If the process includes both surface-mount parts and the TSL202R, the surface mount operations should be completed first with the through-hole parts afterward.

These parts can be washed as a part of the flux cleanup operation. A final top-surface cleanup may be required with water or alcohol to remove any remaining particles.

Ordering & Contact Information

Figure 17:
Ordering Information

Ordering Code	Type	Delivery Form	Delivery Quantity
TSL202R	128 x 1 Array	Tube	25 pcs/tube

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Revision Information

Changes from 032F (2012-Jan) to current revision 1-00 (2016-Jul-25)	Page
Content of TAOS datasheet was converted to the latest **ams** design	
Updated Key Benefits & Features	1
Added Ordering Information	16

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide